Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SOURCE**

**GATE**

**.082”**

**.115”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: G = .018” X .025” S = .024” X .032”**

**Backside Potential: Drain**

**Mask Ref: HEX 2 100V GEN 3**

**APPROVED BY: DK DIE SIZE .082” X .115” DATE: 8/9/17**

**MFG: IR THICKNESS .015” P/N: IRLC120BV**

**DG 10.1.2**

#### Rev B, 7/19/02